HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Juan I. Martinez	Confirmation No.: 3109
Application No.: 10/781,477	Examiner: Riad, Amine
Filing Date: February 17, 2004	Group Art Unit: 2113

Title: System and Method for Reboot Reporting

Mail Stop Appeal Brief - Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF REPLY BRIEF

Transmitted herewith is the Reply Brief with respect to the Examiner's Answer mailed on 03/06/2008 .

This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

(Note: Extensions of time are not allowed under 37 CFR 1.136(a))

(Note: Failure to file a Reply Brief will result in dismissal of the Appeal as to the claims made subject to an expressly stated new ground rejection.)

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Respectfully submitted,

Juan I. Martinez

By: Jed Caven

/Jed Caven Reg. No. 40,551/

Attorney/Agent for Applicant(s)

Reg No. : 40,551

Date : 04/05/2008

Telephone : 720.841.9544

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Juan I. Martinez	)	Group Art Unit: 2113
	)	
Serial No.: 10/781,477	)	Examiner: Riad, Amine
	)	
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For: System and Method for Reboot Reporting

REPLY BRIEF

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated March 6, 2008.

ARGUMENT

I. Rejections Under U.S.C. §102

A. Legal Standard

The standard for lack of novelty, that is, for "anticipation," under 35 U.S.C. §102 is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 231 USPQ 81, 90 (Fed. Cir. 1986). Invalidity for anticipation requires that all of the elements and limitations of the claims be found within a single prior art reference. *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991). Every element of the claimed invention must be literally present, arranged as in the claim. *Richardson v. Suzuki Motor Co.*, 9

USPQ2d 1913, 1920 (Fed. Cir. 1989) (finding that the jury had been erroneously instructed that anticipation may be shown by equivalents, a legal theory that is pertinent to obviousness under Section 103, not to anticipation under Section 102). "The identical invention must be shown in as complete detail as is contained in the patent claim." MPEP §2131 (7th Ed. 1998) (citing *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). Furthermore, functional language, preambles, and language in "whereby," "thereby," and "adapted to" clauses cannot be disregarded. *Pac-Tec, Inc. v. Amerace Corp.*, 14 USPQ2d 1871 (Fed. Cir. 1990).

"It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office." *Ex parte Skinner*, 2 USPQ2d 1788, 1788-1789 (Bd. Pat. Int. 1986) (holding that examiner failed to establish *prima facie* case of anticipation). The examiner has "the burden of proof . . . to produce the factual basis for its rejection of an application under sections 102 or 103." *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) (quoting *In re Warner*, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967)). Only if that burden is met, does the burden of going forward shift to the applicant.

B. Claim 1

Murthy cannot anticipate (or render obvious) independent claim 1 because Murthy neither discloses (nor even suggests) *any* of the limitations recited in independent claim 1. Claim 1 is directed to a method of reboot reporting and recites limitations directed to:

> reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors;
> generating at least one non-maskable interrupt signal;
> outputting the non-maskable interrupt signal to a processor of the plurality of computer systems;
> outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems; and
> generating an indication that at least one computer system has a fault condition.

Contrary to the assertion in the Examiner's Answer, Murthy fails to disclose, or even to suggest, numerous limitations recited in claim 1.

1. Murthy Neither Discloses nor Suggests Reading a Plurality of Input Lines Associated with a Plurality of Computer Systems Having a Plurality of Processors

Claim 1 recites a limitation directed to reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors. The Examiner's Answer asserts that Murthy discloses these limitations, and simply cites Figure 1, items 10A, 10B, 10C, 10D to support the assertion. Applicants disagree, and assert that the citation to Figure 1, items 10A, 10B, 10C, 10D is inadequate to support a *prima facie* case of anticipation.

Contrary to the Examiner's assertion, nothing in the Figure 1, items 10A, 10B, 10C, 10D discloses or suggests reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors, as recited in claim 1. The subject matter of Fig. 1 is an exemplary computer system. At most, Figure 1, items 10A, 10B, 10C, 10D discloses that an exemplary computer system may include a plurality of processors. However, a close inspection of Murthy reveals that Murthy is entirely silent with regard to reboot reporting. Certainly, nothing in Murthy discloses or suggests reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors as described and recited in claim 1. Hence, Murthy cannot anticipate claim 1.

2. Murthy Neither Discloses nor Suggests Generating at least one Non-Maskable Interrupt Signal

Claim 1 further recites a limitation directed to generating at least one non-maskable interrupt signal. The Examiner's Answer asserts that Murthy discloses these limitations, and cites column 2, lines 61-62 to support the assertion. Applicants disagree. The Appeal Brief sets forth in clear and detailed terms the inadequacy of the Examiner's argument. The arguments from the Appeal Brief are incorporated herein, and in the interest of brevity will not be repeated.

3. Murthy Neither Discloses nor Suggests Outputting the Non-Maskable Interrupt Signal to a Processor of the Plurality of Computer Systems

Claim 1 further recites a limitation directed to outputting the non-maskable interrupt signal to a processor of the plurality of computer systems. The Examiner's Answer asserts that Murthy discloses this limitation, and cites column 2, lines 61-62 to support the assertion.

The relevant text reads as follows:

> The problems noted above are solved in large part by a single level interrupt processor on the array controller board that contains a critical failure input line that permits implementation of a nonmaskable pseudo-interrupt for debugging of the array controller. The nonmaskable pseudo-interrupt informs the processor of a debug request even when all device interrupts in the processor are disabled and the array controller board is inoperative. A processor-to-bus bridge connected to the single level interrupt processor on the array controller board contains an interrupt status register, interrupt mask register, and a critical interrupt register. Test equipment is connected to the processor-to-bus bridge through a three pin serial port, the test equipment able to set a bit in the critical interrupt register for requesting the nonmaskable pseudo-interrupt, the processor-to-bus bridge reading the bit in the critical interrupt register to determine whether a nonmaskable pseudo-interrupt has occurred. The processor-to-bus bridge asserts the critical failure input line of the processor after determining that the test equipment has requested the nonmaskable pseudo-interrupt. The processor then executes handler software routines that communicate with the test equipment to debug the array controller board.

Initially, as noted in the arguments submitted in the Appeal Brief, Murthy clearly disavows generating a non-maskable interrupt signal. Thus, Murthy has no non-maskable interrupt signal to be output to a processor of the plurality of the computer systems. Further, the processor referred to in the cited text is the processor 58 on the disk array 50 illustrated in Fig. 2. It is *not* any of the processors 10A, 10B, 10C, 10D asserted by the Examiner's Answer. In short, contrary to the Examiner's assertion, nothing in the cited text discloses or suggests outputting the non-maskable interrupt signal to a processor of the plurality of computer systems, as recited in claim 1. Hence, Murthy cannot anticipate claim 1.

4. Murthy Neither Discloses nor Suggests Outputting the Non-Maskable Interrupt Signal to a Manager Associated with the Plurality of Computer Systems

Claim 1 further recites a limitation directed to outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems. The Examiner's Answer asserts that Murthy discloses this limitation, and cites column 4, lines 18-21 to support the assertion. The relevant text reads as follows:

> Inasmuch as computer system 100 is preferably a server system, the computer system 100 may not have a dedicated display device. If it is desired for the computer system to have a dedicated display device, such a system could be implemented by coupling a video driver card to the host bridge 14 by way of the expansion bus 18 or a separate bus (not shown). If it is desirable for the computer

> system to have a dedicated display device, a video driver or graphic controller would interface the display device to the system. The display may comprise any suitable electronic display device upon which any image or text can be represented.

Initially, Applicant notes that the cited text fails event to mention the structural element of the manger recited in this limitation, much less the operation of outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems as recited in claim 1.

The Examiner's Answer further appears to argue that the disclosure of a display device in Murthy satisfies this limitation. This assertion is wholly without support in the evidence of record. Initially, the manager recited to in the claim refers to the enclosure manager 150 described, *inter alia*, in paragraph [0026] of the application. Thus, a display device is neither necessary nor useful in the operation of outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems as recited in claim 1. Further, the assertions in the Examiner's Answer that the inclusion of a display device satisfies this limitation represent pure conjecture by the Examiner and unsupported by the evidence of record in this application.

5. Murthy Neither Discloses nor Suggests Generating an Indication that at least one Computer System has a Fault Condition

Claim 1 further recites a limitation directed to generating an indication that at least one computer system has a fault condition. The Examiner's Answer asserts that Murthy discloses this limitation, and cites column 2, lines 63-65 to support the assertion. The relevant text reads as follows:

> The problems noted above are solved in large part by a single level interrupt processor on the array controller board that contains a critical failure input line that permits implementation of a nonmaskable pseudo-interrupt for debugging of the array controller. The nonmaskable pseudo-interrupt informs the processor of a debug request even when all device interrupts in the processor are disabled and the array controller board is inoperative. A processor-to-bus bridge connected to the single level interrupt processor on the array controller board contains an interrupt status register, interrupt mask register, and a critical interrupt register. Test equipment is connected to the processor-to-bus bridge through a three pin serial port, the test equipment able to set a bit in the critical interrupt register for requesting the nonmaskable pseudo-interrupt, the processor-to-bus bridge reading the bit in the critical interrupt register to determine whether

> a nonmaskable pseudo-interrupt has occurred. The processor-to-bus bridge asserts the critical failure input line of the processor after determining that the test equipment has requested the nonmaskable pseudo-interrupt. The processor then executes handler software routines that communicate with the test equipment to debug the array controller board..

As noted above, the processor referred to in the cited text is the processor 58 on the disk array 50 illustrated in Fig. 2. It is *not* any of the processors 10A, 10B, 10C, 10D asserted by the Examiner's Answer. Thus, the Murthy neither discloses nor suggests generating an indication that at least one computer system has a fault condition as recited in claim 1.

C. Claim 2

Dependent claim 2 depends from, and further defines over and above claim 1 and by reciting:

> associating the non-maskable interrupt signal with at least one computer system of the plurality of computer systems.

The Examiner's Answer asserts that the Murthy discloses this limitation, and simply cites Figure 1, items 50A, 50B, and 50C to support the assertion. Applicants disagree, and assert that the citation to Figure 1, items 50A, 50B, and 50C is inadequate to support a *prima facie* case of anticipation.

Contrary to the Examiner's assertion, nothing in the Figure 1, items 50A, 50B, and 50C discloses or suggests associating the non-maskable interrupt signal with at least one computer system of the plurality of computer systems, as recited in claim 2. The subject matter of Fig. 1 is an exemplary computer system. At most, Figure 1, items 50A, 50B, and 50C discloses that an exemplary computer system may include a plurality of array controllers. However, a close inspection of Murthy reveals that Murthy is entirely silent with regard to reboot reporting. Certainly, nothing in Murthy discloses or suggests associating the non-maskable interrupt signal with at least one computer system of the plurality of computer systems as described and recited in claim 2. Hence, Murthy cannot anticipate claim 2.

D. Claim 3

Dependent claim 2 depends from, and further defines over and above claim 2 by reciting:

> generating a notice identifying the at least one computer system.

The asserts that Murthy discloses these limitations, and cites column 6, lines 46-52 to support the assertion. Appellants disagree. The cited text reads as follows:

> This nonmaskable pseudo-interrupt workaround permits debugging even if all interrupts in processor 58 have been disabled and a hardware failure has occurred on the array controller board 50 which has completely "hung" the system (i.e. the array controller board is inoperative and not responding) so that no onboard debug fault tolerance features can correct the problem.

Contrary to the Examiner's assertion, nothing in the cited text discloses or suggests generating a notice identifying the at least one computer system, as recited in claim 3. The Examiner's Answer argues that "debugging with the NMI means first that the item to be debugged is identified before starting the debugging." Again, this argument is pure conjecture and unsupported by the evidence. Further, the nonmaskable pseuo-interrupt signal described in Murthy relates to the processors 58 in the array controllers 50A, 50B, 50C, and are completely unrelated to any of the processors 10A, 10B, 10C, 10D, in the computer systems. Hence, Murthy cannot anticipate claim 3.

E. Claim 4

Dependent claim 4 depends from, and further defines over and above claim 3 by reciting:

:

> redistributing the processing load from the at least one computer system to the remaining plurality of computer systems.

The asserts that Murthy discloses these limitations, and cites column 8, lines 17-21 to support the assertion. Appellants disagree. The cited text reads as follows:

> Overall system availability and reliability is increased because of the compartmentalized nature of the debug hardware and software that permits one array controller board to be debugged without effecting the remainder of

computer system 100.

Contrary to the Examiner's assertion, nothing in the cited text discloses or suggests redistributing the processing load from the at least one computer system to the remaining plurality of computer systems, as recited in claim 4. The Examiner's Answer argues that "because the remainder of system 100 is not effected it means that the system has a redistribution system in case a fault happens in one of its elements." Again, this argument is pure conjecture and unsupported by the evidence. Hence, Murthy cannot anticipate claim 4.

F. Claim 5

Dependent claim 5 depends from, and further defines over and above claim 1 and by reciting:

> counting the number of times the non-maskable interrupt signal is generated.

The final Action cited The Examiner's Answer asserts that Murthy discloses these limitations, and cites column 6, lines 36-39 to support the assertion. Appellants disagree. The cited text reads as follows:

> In addition to the host bridge device 14, the computer system 100 also includes another bridge logic device 22 that bridges the primary expansion bus 18 to various secondary buses including a low pin count ("LPC") bus 24 and a peripheral component interconnect ("PCI") bus 20 (referred to as the "host" PCI bus).

Contrary to the Examiner's assertion, nothing in the cited text discloses or suggests counting the number of times the non-maskable interrupt signal is generated, as recited in claim 4. The Examiner's Answer argues that "Examiner considers the LPC as a pin that counts the NMIs." Again, this assertion is pure conjecture and wholly unsupported by the evidence in Murthy. Hence, Murthy cannot anticipate claim 5.

G. Claim 6

Murthy cannot anticipate (or render obvious) independent claim 6 because Murthy neither discloses (nor even suggests) *any* of the limitations recited in independent claim 6. Claim 6 is directed to a system for reboot reporting and recites limitations directed to:

> a plurality of computer systems having at least one processor and at least one non-maskable interrupt output;
>
> a manager system in circuit communication with the plurality of computer systems and comprising at least one non-maskable interrupt input associated with the plurality of computer systems.

Contrary to the assertion in the Examiner's Answer, Murthy fails to disclose, or even to suggest, the limitations recited in claim 6.

1. Murthy Neither Discloses nor Suggests a Plurality of Computer Systems Having at least one Processor and at least one Non-Maskable Interrupt Output

Claim 6 recites a limitation directed to a plurality of computer systems having at least one processor and at least one non-maskable interrupt output. The Examiner's Answer asserts that Murthy discloses these limitations, and cites column 2, lines 18-21 to support the assertion. In addition, the Examiner's Answer asserts the same argument applied to claim 1. Applicants disagree. As described above, items 50A, 50B, and 50C depicted in Fig. 1 refer to disk array controllers, which are described with particularity with reference to item 50 in Fig. 2. Further, the cited text reads as follows:

> The nonmaskable pseudo-interrupt informs the processor of a debug request even when all device interrupts in the processor are disabled and the array controller board is inoperative.

Initially, as noted in the arguments submitted in the Appeal Brief, Murthy clearly disavows generating a non-maskable interrupt signal. Thus, Murthy has no non-maskable interrupt signal to be output from a processor of the plurality of the computer systems. Further, the processor referred to in the cited text is the processor 58 on the disk array 50 illustrated in Fig. 2. It is *not* any of the processors 10A, 10B, 10C, 10D asserted by the Examiner's Answer. Further, the processor 58 on the disk array 50 does not generate our output a non-maskable interrupt signal. In short, contrary to the Examiner's assertion, nothing in the cited text discloses or suggests a plurality of computer systems having at least

one processor and at least one non-maskable interrupt output, as recited in claim 6.

2. Murthy Neither Discloses nor Suggests a Manager System in Circuit Communication with the Plurality of Computer Systems and Comprising at least one Non-Maskable Interrupt Input Associated with the Plurality of Computer Systems

Claim 6 further recites a limitation directed to a manager system in circuit communication with the plurality of computer systems and comprising at least one non-maskable interrupt input associated with the plurality of computer systems. The Examiner's Answer asserts that Murthy discloses these limitations, and cites column 2, lines 61-62 to support the assertion. In addition, the Examiner's answer asserts the same argument applied to claim 1, namely that the inclusion of a display device in Murthy reads on this limitation.

Applicants disagree. This issue is addressed in section B.4, above. As set forth above, Murthy lacks any structure corresponding to the manager system recited in claim 6. Further, the assertions in the Examiner's Answer represent pure conjecture by the Examiner and unsupported by the evidence of record in this application.

H. Claims 7-12

Claims 7-12 address various features of the manager system recited in claim 6. Murthy cannot anticipate (or render obvious) dependent claims 7-12 because, as set forth above, Murthy lacks any structure corresponding to the manager system recited in various of claims 7-12. Further, the assertions in the Examiner's Answer that the display device necessitates the inclusion of a management system represent pure conjecture by the Examiner and unsupported by the evidence of record in this application.

I. Claims 13-19

Claims 13-18 stand or fall with claim 1. Claim 19 stands or falls with claim 5.

J. Claims 20-21

Claims 20-21 stand or fall with claim 1.

K. Claims 22-25

Claims 22-25 stand or fall with claim 1.

L. Claims 26-30

Claims 26-28 and 30 stand or fall with claim 1.

Claim 29 stands or falls with claim 4.

CONCLUSION

Murty fail to disclose or suggest limitations of appellants' claims. Therefore, the cited cannot be used to establish the required *prima-facie* case of anticipation under 35 U.S.C. §102. Accordingly, Appellants urge the Board to reverse the examiner's rejections of the pending claims.

Respectfully submitted,

Jed W. Caven
Caven & Aghevli LLC
Attorney for Applicants

/Jed W. Caven/

By:
Jed W. Caven
Registration No. 40,551
(720) 841-9544

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